

ISSUE CLASSIFICATION	
Class	Subclass

N-P

PATENT NUMBER

U.S. **UTILITY** Patent Application

<p>O.I.P.E.</p> <p>SCANNED <i>[Signature]</i> Q.A. <i>[Signature]</i></p>	<p>PATENT DATE</p>
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APPLICATION NO. 09/972011	CONT/PRIOR D	CLASS 257 716	SUBCLASS 125	ART UNIT 2841200	EXAMINER Rossoshak
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## APPLICANTS

Steven Teig  
Andrew Caldwell

**TITLE**

Method and arrangement for layout and manufacture of nonmanhattan semiconductor integrated circuit using simulated euclidean wiring

PTO-2040  
12/99

## ISSUING CLASSIFICATION

ORIGINAL				CROSS REFERENCE(S)								
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)							
INTERNATIONAL CLASSIFICATION												

☐ Continued on Issue Slip Inside File Jacket

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>		<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)		<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____ _____ _____	_____ (Primary Examiner) (Date)		<b>ISSUE FEE</b>	
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